



“Techno-Social Excellence”
Marathwada Mitramandal's
INSTITUTE OF TECHNOLOGY (MMIT)
Lohgaon, Pune-411 047



“Towards ubiquitous Computing Technology”
Department of Computer Engineering

Term End Exam

Programme: SE

Semester: II

Course Code: 210253

Course Name: Microprocessor

Branch: Computer Engineering

Academic Year: 2019-20

Duration: 1 Hour

Max Marks: 30

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Student PRN No.

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Student Roll No.

Instructions:

Questions are of MCQs type. Question paper will be as per the format

- a) Maximum Marks- 50 questions
- b) Total question –25
- c) 1 Mark MCQ-16question
- d) 2 Marks MCQ/short questions – 11 questions
- e) 4 Marks MCQ/short answer questions – 03questions.
- f) For numerical based subject 2MarksMCQis also based on short numerical.

1. What is the size of an Interrupt Gate descriptor located in IDT of a logic gate is 1 when all its inputs are logic
The gate is either [1 M]
 - a) 64 KB
 - b) 8 byte
 - c) 1 MB
 - d) 32 bit

2. Task Gate ,Interrupt Gate , Trap Gate descriptors are located in ?m [1 M]

- A] IDT (Interrupt Descriptor Table)
- B] GDT (Global Descriptor Table)



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C] LDT (Local Descriptor Table)
D] Task Register

3. Maskable interrupts are signalled via. [1 M]

- a) INTR pin
- b) INT pin
- c) NMI pin
- d) BUSY pin

4. When IF(Interrupt Flag) is disabled following is true? [1 M]

- a) Procedures are disabled
- b) Multitasking is disabled
- c) INTR interrupts are disabled
- d) Macros are disabled

5. What is stored in Interrupt Gate Descriptor. [1 M]

- a) Selector to segment descriptor of Interrupt Procedure segment
- b) Offset within segment of Interrupt procedure segment
- c) DPL of Interrupt Gate descriptor
- d) All of the above

6. The test register(s) that is provided by 80386 for page cacheing is? [1 M]

- a) test control registers
- b) page cache registers
- c) test control and test status registers
- d) test control and page cache registers

7. Among eight debug registers, DR0-DR7, the registers that are reserved by Intel are[1 M]

- a) DR0, DR1, DR2
- b) DR4, DR5
- c) DR1, DR4
- d) DR5, DR6, DR7

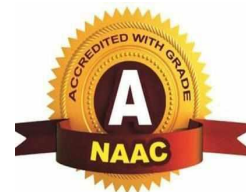
8. The registers that are used to store four program controllable break point addresses are[1 M]

- a) DR5-DR7
- b) DR0-DR1
- c) DR6-DR7
- d) **DR0-DR3**

9. The register DR6 hold

[1 M]

- a) break point status
- b) break point control information



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- c) break point status and break point control information
- d) none of the mentioned

10. The flag bits that indicate the privilege level of current IO operations are [1 M]

- a) virtual mode flag bits
- b) IOPL flag bits
- c) resume flag bits
- d) none of the mentioned

11. The registers that are not available for programmers are [1 M]

- a) data and address registers
- b) instruction pointers
- c) segment descriptor registers
- d) flag registers

12. The flag that is additional in flag register of 80386, compared to that of 80286 is [1 M]

- a) VM
- b) RF
- c) VM, RF
- d) None of the mentioned

13. The VM (virtualmode) flag is to be set, only when 80386 is in [1 M]

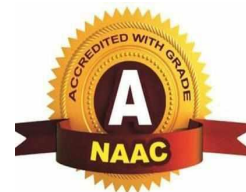
- a) Virtual Mode
- b) protected mode
- c) either virtual or protected mode
- d) all of the mentioned

14. In protected mode of 80386, the VM flag is set by using [1 M]

- a) IRET instruction
- b) Task switch operation
- c) IRET instruction or task switch operation
- d) None of the mentioned

15. During the instruction cycle of 80386, any debug fault can be ignored if [1 M]

- a) VM flag is set
- b) VM flag is cleared



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- c) RF is cleared
- d) RF is set

16. The RF is not automatically reset after the execution of [1 M]

- a) IRET
- b) POPA
- c) IRET and POPF
- d) IRET and PUSHF

17. If the 80386 enters the protected mode from the real address mode, then it returns back to the real mode, by performing the operation of? [2 M]

- a) Read
- b) write
- c) terminate
- d) reset

18. The unit that is needed for virtual mode 80386, only to run the 8086 programs, which require more than 1 Mbyte of memory for memory management functions, is. [2 M]

- a) execution unit
- b) central processing unit
- c) paging unit
- d) segmentation unit

19. The 80386DX is a processor that supports [2 M]

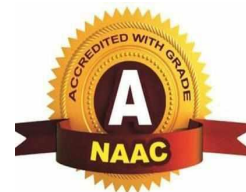
- a) 8-bit data operand
- b) 16-bit data operand
- c) 32-bit data operand
- d) all of the mentioned**

20. The 80386DX has an address bus of [2M]

- a) 8 address lines
- b) 16 address lines
- c) 32 address lines
- d) 64 address line

21. 80386DX is available in a grid array package of [2M]

- a) 64 pin
- b) 128 pin



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- c) 132 pin
- d) 142 pin

22. The operating frequency of 80386DX is [2M]

- a) 12 MHz and 20 MHz
- b) 20 MHz and 33 MHz
- c) 32 MHz and 12 MHz
- d) all of the mentioned

23. Which of the following pin when activated, allows address pipelining? [2M]

- a) ADS
- b) NA
- c) AP
- d) None of the mentioned

24. The signal that is used to insert WAIT states in a bus cycle in 80386 is [2M]

- a) HOLD
- b) HLDA
- c) READY
- d) PEREQ

25. The signal which indicates to the CPU, to fetch a data word for the coprocessor is

- a) READY
- b) NMI
- c) HLDA
- d) PEREQ

26. The instruction that stores a copy of top of the stack into the memory, and pops the top of the stack is [2M]

- a) FST
- b) FSTP
- c) FIST
- d) FLD



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27. If the result is infinity, then the exception generated is [2M]

- a) overflow
- b) invalid operation
- c) denormalized operand
- d) zero divide

28. If the result is rounded according to the rounding control bits, then the exception generated is

- a) denormalized operand [4M]
- b) underflow
- c) inexact result
- d) invalid operation

29. The exception generated for a too big result to fit in the format is [4M]

- a) invalid operation
- b) overflow
- c) denormalized operand
- d) result overflow

30. Invalid operation is the exception generated due to [4M]

- a) stack overflow
- b) stack underflow
- c) indeterminate form as result
- d) all of the mentioned