



Stream

Classwork

People

Grades

All topics



Create



MP Insem Exam

Posted Jun 10, 2021

MP_Lecture 2

Posted Jan 22, 2021

Addressing mode

Posted Jan 22, 2021

MP I Lecture PPT

Posted Jan 22, 2021

MP oral



MP Oral Question Bank

Posted Jun 12, 2021

Continuous Assessment



Students will see this topic once work is added to it

Virtual Lab





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Assignment



Draw diagram 1.Format of 80386 TSS 2...	Due May 24, 2021, 11:59 ...
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Assignment No. 7 1.Draw Diagram of P...	Due May 18, 2021, 11:59 ...
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Assignment No. 6 Draw table of CPL,RP...	Due May 19, 2021
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Assignment no. 5 Draw Diagram:-1. Pri...	Due May 18, 2021, 11:59 ...
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Ass 3 Draw Diagram of 80386 Register...	Due Mar 2, 2021, 11:59 PM
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Ass 4 Draw Interrupt & Exceptions tabl...	Due Feb 20, 2021, 11:59 ...
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Ass NO. 1	Due Jan 23, 2021, 11:59 ...
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Ass2 Draw Pin diagram of 80386	Due Feb 9, 2021, 11:59 PM
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Quiz Assignment



Quiz 10 Logical Insructions	Due Mar 31, 2021, 11:59 ...
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Quiz 7 Application Instruction Set	Due Jun 1, 2021, 11:59 PM
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Quiz 5_Basics of Microprocessor	Due May 30, 2021, 11:59 ...
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Quiz 4 System Registers

Due Jun 2, 2021, 11:59 PM

MP-Test I

Due May 31, 2021, 11:59 ...

Quiz 11

Due May 31, 2021, 11:59 ...

Quiz 14 Control Register

Due Jun 1, 2021, 11:59 PM

Quiz 6 Basic Programming model 80386

Due May 31, 2021, 11:59 ...

View more

Syllabus



Syllabus

Posted Mar 22, 2021

Theory Assignment



Unit 1 -Assignment No. 1

Due Mar 14, 2021, 11:59 ...

Assignment Theory

Edited Mar 20, 2021

E-Book



PPT



Unit 1 Part 2	Edited Mar 23, 2021
Unit part 1	Edited Mar 23, 2021
pin diagram of 80386 & Register Orga...	Edited Mar 23, 2021
Lecture 1,2 PPT	Edited Mar 23, 2021
Unit 6	Posted Mar 20, 2021
Unit 5	Posted Mar 20, 2021
Unit 4	Edited May 13, 2021
Unit 3	Posted Mar 20, 2021
Unit 2	Posted Mar 20, 2021
Unit 1	Edited Mar 20, 2021

SPPU Question Paper



University Question Paper

Edited Mar 20, 2021



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Hand written Notes

Edited Mar 20, 2021

Attendance



SE-A Attendance

Posted Mar 20, 2021

Attendance

Posted Mar 20, 2021

Unit Test



RETEST Unit TEST II MP

Due Mar 30, 2021, 4:00 PM

MP Unit Test II

Due Mar 23, 2021, 2:30 PM

MP Video



Video lecture link

Edited Mar 23, 2021





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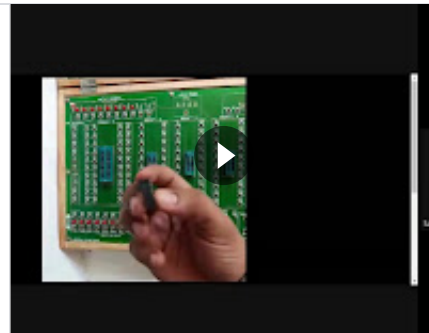


New

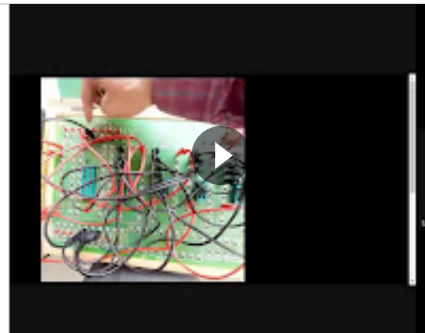
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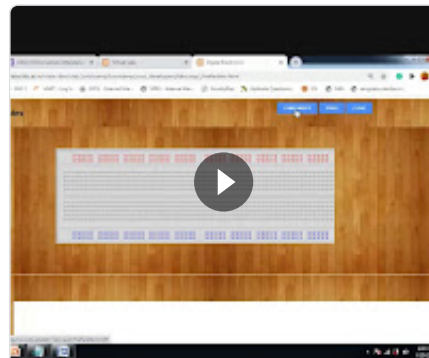
Shared with me > ... > PRACTICAL > DEL



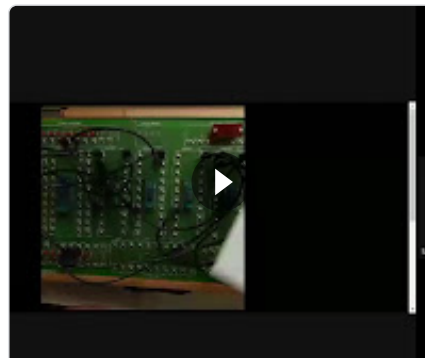
1_Working of Digital Kit_29 June_1:...



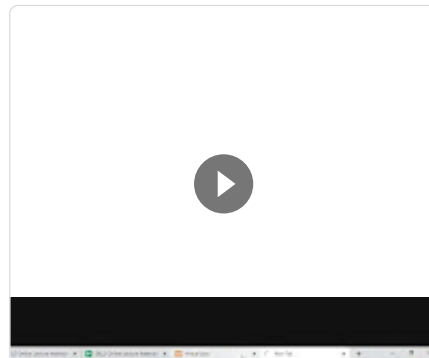
2_Implementation fo AdderSub_13 ...



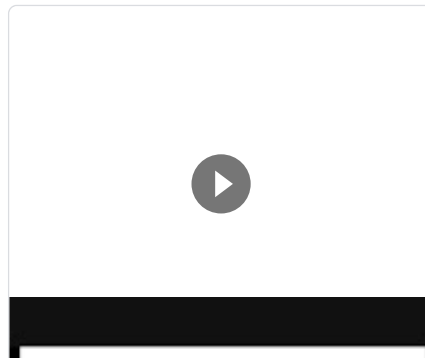
3_Gray to Binary_VLab_20 July_1:30...



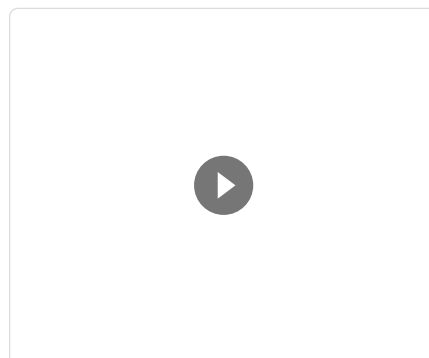
4_Implementation of code converto...



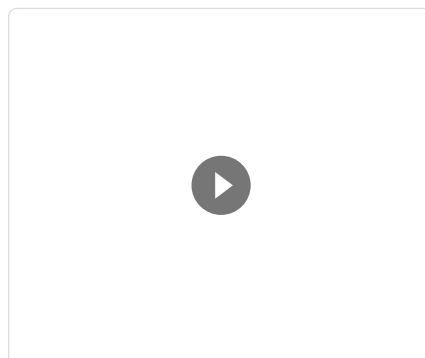
5_Implementation of BCD adder_3 A...



6_Implementation of Parity_10 Aug_...



7_Implementation of MUX_17 Aug_...



8-Implementation of Comparator & ...



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- Unit No. 3
- Unit No. 4
- Unit No. 5
- Unit No. 6



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Practical:

Savitribal Pralokh University
Second Year of Computer Engineering (2018 Course)
21124K (Digital Logic) 140014019

Teaching Scheme: 180 Hours/Week Examination Scheme: 20 Marks

1W Assessment :

- Continuous assessment of laboratory work is done based on overall performance and Laboratory performance of student.
- Assessment includes- timely completion, performance, innovation, efficiency, punctuality and neatness.

1_Logic Gates_2 June_10am.mp4

Example 2

Convert the expression into standard form:

$$Y = A + BC + \bar{A}BC$$

2_IC & Logical Expression_9 June_1...

Table:

Decimal	Signed Magnitude	Signed One's Complement	Signed Two's Complement
+4	0100	0100	0100
+3	0011	0011	0011
+2	0010	0010	0010
+1	0001	0001	0001
+0	0000	0000	0000
-1	1001	1100	1111
-2	1010	1101	1110
-3	1011	1100	1101
-4	1100	1011	1100

3_SOP POS_Complements_16 June...

Objectives

- To study the basic concept of K- map technique
- To minimize the logical function using K- map technique

Unit 1: Minimization Technique (26 Hours)

Logic Design Minimization Technique - Minimization of Boolean function using 4-map to 4 variables and Quine McCluskey Method. Representation of signed number- sign, magnitude representation. 2's complement and 1's complement form (not needed) can be reviewed. Sum of product and Product of sum form. Minimization of SOP and POS using K-map.

Minimize/Case studies: Digital logic using logic gates

4_Introduction to K-Map_17 June_1...

Video thumbnail for K-map Example (Part-1)

5_K-map Example(Part-1)_23 June...

Video thumbnail for K-map Example (Part-2)

6_K-map Example(Part-2)_24 June...

Video thumbnail for Dont Care Condition

7_Dont Care Condition_30 June_10...

Video thumbnail for Quine McCluskey (Part-1)

8_Quine McCluskey(Part-1)_7 July...